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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/989,571	11/19/2001	Manfred Bartz	CYPR-CD01168M	1215

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EXAMINER	
DIMYAN, MAGID Y	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/989,571	BARTZ ET AL.	
	Examiner	Art Unit	
	Magid Y Dimyan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/18/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Acknowledgement

1. Receipt is acknowledged of the Amendments to the Claims, Amendments to the Specifications, Remarks, and Formal Drawings, all filed on October 18, 2004. It is also acknowledged that the Applicants have amended claims 1, 9 and 16. Claims 1 – 20 remain pending in this Application.

Specification

2. The disclosure is objected to because of the following informalities: On page 12 - line 13, page 14 - line 6, and page 17 - line 18, the U.S. Patent Application Serial Numbers are missing.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1, 9 and 16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The Specification doesn't refer to, or describe the elements "valid position overlays a portion of said resources represented in said graphical user interface (claim 1)" or "allowable position graphically overlays a portion of said layout of resources" (claim 9), or "allowable position overlaying at least one of said resource images" (claim 16).

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1, 9 and 16 recite the limitations "valid positions overlays a portion of said resources" (claim1), "allowable position graphically overlays a portion of said layout of resources" (claim 9), and "allowable position overlaying at least one of said resource images" (claim 16). There is insufficient antecedent basis for these limitations in the claims.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1 – 6 and 8 – 19 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,449,761 to Greidinger et al. (hereinafter, "Greidinger").

9. Referring to claim 1, Greidinger discloses a method of designing a circuit for a device comprising: (a) selecting a first module of a plurality of modules, the module representing predetermined functions operable to be implemented in resources in the device (see Fig. 9A; column 9, lines 40 – 60); and (b) placing the first module in a valid position in a GUI, wherein the resources are represented in a Graphical User Interface (GUI) and wherein the valid position depends upon the type of module being placed and the characteristics of the resources (see Figs. 9A, 12A1 – 12H2; col. 5, line 57 to col. 8. line 65); wherein the valid position overlays a portion of the resources represented in the GUI (see also Fig. 3; col.

6, lines 3 – 49, and Fig. 6; col. 7, line 64 – col. 8, line 45). Thus, Greidinger cites all the elements of the claim.

10. As per claims 2 and 3, see (5) above, as well as col. 3, line 37 to col. 4, line 10 and col.5, lines 20 – 44, which teach how the additional modules are selected, and how they can be moved to a new valid position using a GUI, as claimed.

11. As for claim 4, see (5) and (6) above, as well as Figs. 2 and 3, which recite how the resource images are mapped in the GUI as claimed.

12. Referring to claims 5 and 6, see (5) and (6) above, as well as Fig. 9A, blocks 902, 906 and 908; col. 9, lines 33 – 65; which show how the I/O pins of the modules, and the module parameters, are selected from a window, as claimed.

13. As per claim 8, see (5) above, as well as Fig. 9A, block 902, which cite the inclusion of programmable digital and analog blocks (PLL, A/D, AGC, CPU, Memory, etc) in the design, as claimed.

14. As for claim 9, see (5) – (8) above, which teach the same elements of: (a) selecting and placing modules in a GUI based on the module characteristics, wherein allowable position graphically overlays a portion of the layout resources;

(b) iterating the process to place additional modules; and (c) selecting pin configurations.

15. Referring to claims 10 and 11, see (10) above, as well as Figs. 3 and 4; col.3, line 3 to col. 7, line 33, which disclose how the modules can be moved to new valid positions based on module characteristics, as claimed.

16. Referring to claim 12, see (10) above, as well as Fig. 4, which show how modules of one class (block 326A) can be moved to a new position, while modules of a second class (block 322B) are kept in the same position as claimed.

17. Claim 13 contains the same limitations as claims 4 and 5, and therefore the same rejections apply.

18. As per claims 14 and 15, see Fig. 9A, block 902 and col. 9, line 52, which show a CPU used in the design. A CPU can be programmed to perform predetermined functions by editing a source code. Also shown in Fig. 9A are the global parameters related to global resources of the circuit, as claimed.

19. Claim 16 contains the same elements found in claims 9 and 13, and thus the same rejections apply.

20. As per claim 17, see Fig. 3, which shows how modules can be moved to a new position in a GUI, as claimed.

21. Referring to claim 18, see above; Fig. 9A; col. 9, lines 40 – 60, which describe the pin configuration selection process, as claimed.

22. As per claim 19, see Figs. 11A – 11C and 12A1 – 12 J, which cite how the interconnections are made between the placed modules, as claimed.

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claims 7 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Greidinger in view of U.S. Patent No. 5,930,148 to Bjorksten et al. (hereinafter, "Bjorksten").

25. Referring to these claims, the teachings of Greidinger pertaining to a method of designing a circuit using modules representing pre-determined functions and placing these modules via a GUI are cited above. However, Greidinger does not disclose the use of an application program interface (API) in

his invention. On the other hand, Bjorksten teaches a method and system for design verification that contains layout software interfaced to an operating system via a GUI and an API (see Fig. 2; col. 3, lines 25 – 45). Since API are now commonly used to interface between design/simulation/layout tools, and high-level programming languages such as Verilog, C++, VHDL, etc, it would therefore be obvious to one having ordinary skill in the art at the time of the invention to combine the teachings of Greidinger and Bjorksten to obtain the same claimed invention.

Response to Arguments

26. Applicant's arguments filed October 18, 2004 have been fully considered but they are not persuasive. As cited above, Greidinger discloses a method and system for designing a circuit for a device that includes selecting a first module of a plurality of modules, the modules representing pre-determined functions (see also Figs. 3 and 4); and placing module in a valid position using a GUI (see also Figs. 6 – 9). The Applicants argue that Greidinger does not teach the added new elements in claims 1, 9 and 16 pertaining to the "valid or allowable positions of the modules overlaying a portion of resources". However, as indicated above, the Examiner has been able to find these elements cited by Greidinger as indicated above. The rejections of all the claims are therefore maintained.

27. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y Dimyan whose telephone number is (571) 272-1889. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on (571) 272-1907.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Magid Y Dimyan
Examiner
Art Unit 2825

myd
12 January 2005

MYD

VUTHE SIEK
PRIMARY EXAMINER